High-Throughput VLSI Architecture for GRAND Markov Order

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Abstract—Guessing Random Additive Noise Decoding (GRAND) is a recently proposed Maximum Likelihood (ML) decoding technique. Irrespective of the structure of the error correcting code, GRAND tries to guess the noise that corrupted the codeword in order to decode any linear error-correcting block code. GRAND Markov Order (GRAND-MO) is a variant of GRAND that is useful to decode error correcting code transmitted over communication channels with memory which are vulnerable to burst noise. Usually, interleavers and de-interleavers are used in communication systems to mitigate the effects of channel memory. Interleaving and de-interleaving introduce undesirable latency, which increases with channel memory. To prevent this added latency penalty, GRAND-MO can be directly used on the hard demodulated channel signals. This work reports the first GRAND-MO hardware architecture which achieves an average throughput of up to 52 Gbps and 64Gbps for a code length of 128 and 79 respectively. Compared to the GRANDAB, hard-input variant of GRAND, the proposed architecture achieves 3 dB gain in decoding performance for a target FER of 10^{-5} . Similarly, comparing the GRAND-MO decoder with a decoder tailored for a (79,64) BCH code showed that the proposed architecture achieves 33% higher worst case throughput and 2 dB gain in decoding performance.

Index Terms—Guessing Random Additive Noise Decoding (GRAND), Guessing Random Additive Noise Decoding Markov Order (GRAND-MO), maximum likelihood decoding (MLD), Burst Errors, Low Latency, VLSI architecture.

I. INTRODUCTION

For 5G and beyond communication networks, ultra-reliable low-latency communication (URLLC) [1] is a very promising addition to the pre-existing communication standards [2]. URLLC enables many applications such as augmented and virtual reality, intelligent transportation systems (ITA) [3], internet of things (IoT) [4], [5], machine to machine communication and many others [6]. Realizing these applications requires short high-rate maximum likelihood performing codes to support the low latency and high reliability requirements of mission critical events. For such codes, GRAND has been developed as a maximum likelihood (ML) decoding algorithm [7]. GRAND attempts to guess the noise that corrupted the transmitted codeword rather than decoding the received vector by leveraging the structure of the underlying code. This makes GRAND a desirable code agnostic decoder as it can be used to decode any linear block code. GRAND relies on the generation of putative test error patterns that are successively applied to the received vector. The order in which these putative test error patterns are generated is the key difference between different

variants of GRAND. There are hard-input variants of GRAND (GRANDAB) [7] as well as soft-input variants (ORBGRAND [8], SRGRAND [9], SGRAND [10]). GRAND Markov Order (GRAND-MO) [11] is a hard-input GRAND variant designed specifically for channels with memory which are susceptible to burst noise. Due to the effect of burst noise, channels with memory suffer from a significant degradation in decoding performance with typical channel code decoders, and this degradation increases with channel memory [11]. As a result, interleavers/deinterleavers are used to mitigate the effects of burst noise in order to reduce performance degradation. Interleavers and deinterleavers, on the other hand, introduce additional latency. In emerging applications such as URLLC [1]-[6], where latency and reliability are critical, the delay imposed by interleavers/de-interleavers or the performance degradation caused by channel memory is unacceptable. GRAND Markov Order (GRAND-MO) [11] eliminates the need for interleavers/deinterleavers for channels with memory, allowing for effective and reliable communication in the presence of burst noise. GRAND-MO makes use of noise correlations and adapts its test error pattern generation to mitigate the effect of noise bursts. As a result, GRAND-MO outperforms traditional channel code decoders in the presence of burst noise.

The complexity of GRAND-MO, defined as the maximum number of codebook membership queries done, is directly proportional to the number of putative test error patterns. In this paper, we propose a novel method for generating test error patterns to reduce the complexity of GRAND-MO decoding. Furthermore, we propose the first hardware architecture for GRAND-MO. Considering a code of length 128 and a target FER of 10^{-5} , the proposed architecture achieves an average throughput of 52 Gbps, and outperforms GRANDAB [12] by 3 dB. As compared to the (79, 64) BCH code decoder [13], the proposed VLSI architecture provides 33% higher worst-case throughput and a 2 dB gain for a target FER of 10^{-5} .

The rest of this paper is organized as follows: Section 2 describes the GRAND-MO algorithm and the channel model under consideration. Section 3 introduces complexity reduction techniques for GRAND-MO and their use to develop the proposed hardware architecture. Additionally, Section 3 presents a comparison of the proposed GRAND-MO architecture with GRANDAB and a newly developed BCH decoder. Finally, in Section 4, concluding remarks are made.

II. PRELIMINARIES

A. Notations

Matrices are denoted by a bold upper-case letter (M), while vectors are denoted with bold lower-case letters (v). The transpose operator is represented by \top . The number of k-combinations from a given set of n elements is noted by $\binom{n}{k}$. $\mathbb{1}_n$ is the indicator vector where all locations except the n^{th} location are 0 and the n^{th} location is 1. All the indices start at 1.

B. Channel Model

In this work, the classic two-state Markov chain [14] is used to model a binary channel with burst noise. When the channel is in a good state, G, the channel is noiseless; however, when the channel is in a bad state, B, the channel becomes noisy and introduces errors. The transition probability from G to B is b, and the transition probability from B to G is g. Both b and gare assumed to be known and, in practice, can be estimated. A burst error is a sequence of consecutive errors introduced by the channel, with a length that follows a geometric distribution of mean $\frac{1}{g}$ and variance $\frac{1-g}{g^2}$. The Markov channel's stationary bit-flip probability p is $\frac{b}{b+g} = Q(\sqrt{2R\frac{E_b}{N_0}})$ where R is the code rate. It should be noted that when p = b, the Markov channel transforms into a memoryless BSC.

C. GRAND Markov Order

Algorithm 1 summarizes GRAND-MO's pseudo-code for a linear (n, k) block code, where n is the code length and k is the number of information bits. The algorithm's inputs are r, b, g and $\lfloor \frac{d}{2} \rfloor$ where r is the received vector of size n and d is the minimum distance of the code. Moreover, the algorithm also utilizes the $(n - k) \times n$ parity check matrix H of the code and the $n \times k$ matrix G^{-1} , with G being the generator matrix of the code $(G^{-1} \cdot G = I)$.

The error vector is initialized to 0 (line 1) in GRAND-MO, and Δl is computed using b and g (line 2). Then, the test error patterns are generated sequentially by referring to Δl (line 4). The generated error patterns have m bursts and have a Hamming weight of l. Finally, r is combined with the current test error pattern, and the resulting word is queried for codebook membership by verifying that

$$\boldsymbol{H} \cdot (\boldsymbol{r} \oplus \boldsymbol{e})^{\top} \tag{1}$$

is equal to zero. If the resulting codeword belongs to the codebook, the message (\hat{u}) is recovered (line 7). GRAND-MO decoding is terminated when the number of bursts m in the generated test error pattern and the Hamming weight l of the error pattern equal $\lfloor \frac{d}{2} \rfloor$.

The frame error rate (FER) performance for GRAND-MO decoding of BCH code (127, 106) in Markov channels is plotted in Fig. 1. The demodulator provides hard decision values to the GRAND-MO decoder. It is noted that GRAND-MO's performance improves as channel memory increases (*g*)

Algorithm 1: GRAND Markov Order Input: $H, G^{-1}, r, b, g, \lfloor \frac{d}{2} \rfloor$ Output: \hat{u} OR ABANDON 1 $e \leftarrow 0$ 2 $\Delta l \leftarrow \lfloor \frac{\log(\frac{b}{g})}{\log(\frac{1-g}{1-b})} \rfloor$ 3 while $H \cdot (r \oplus e)^{\top} \neq 0$ do 4 $\begin{bmatrix} [e, m, l] \leftarrow \\ generateNewMarkovErrorPattern (\Delta l) \end{bmatrix}$ 5 $\begin{bmatrix} m = = \lfloor \frac{d}{2} \rfloor AND \ l = = \lfloor \frac{d}{2} \rfloor \\ return ABANDON \end{bmatrix}$

7 $\hat{m{u}} \leftarrow (m{r} \oplus m{e}) \cdot m{G}^{-1}$

8 return \hat{u}



Fig. 1. Comparison of the GRAND-MO and BCH Berlekamp-Massey (B-M) decoding performance of BCH code (127, 106) in Markov channels.



Fig. 2. Comparison of the GRANDAB (AB = 3) and GRAND-MO decoding performance using RLC code (128, 104) with Markov query order and proposed query order (g, m, l_1, l_2).

decreases), while the traditional BCH Berlekamp-Massey (B-M) decoder [15], [16] shows a degradation in FER performance with the increase in channel memory. GRAND-MO's performance differs from that of the BCH decoder because



Fig. 3. Test error pattern generation for GRAND-MO for n = 6 and $\Delta l = 2$ (a) Upper: Markov query order (b) Middle: Proposed re-arranged query order (c) Bottom: Proposed query order with parameters (m = 2, $l_1 = 4$ and $l_2 = 3$).



Fig. 4. Comparison of the GRAND-MO (g = 0.2) decoding performance using BCH code (127, 106) with Markov query order and proposed query order with parameters (m, l_1 , l_2).

GRAND-MO adjusts its error pattern generation to mitigate the impact of noise bursts in the channel.

Similar trends can be observed with Random Linear Codes (RLCs). RLCs are linear block codes that are theoretically known to be high-performing [17], [18], but not considered practical in terms of decodability. Fig. 2 plots the FER performance for GRAND-MO and GRANDAB [7] decoding of RLCs of length n = 128. We can observe that with the decrease in g, GRAND-MO outperforms GRANDAB (AB = 3) decoder in FER performance.

III. VLSI ARCHITECTURE FOR GRAND-MO

We describe the proposed VLSI architecture for GRAND-MO decoding in this section. Furthermore, we analyse the error patterns generated by GRAND-MO and suggest simplifications to the test pattern generation process.

A. Test error pattern generation for GRAND-MO

GRAND-MO generates test error patterns in Markov query order. Fig. 3 (a) depicts the Markov query order for code length n = 6 and $\Delta l = 2$ where each column corresponds to a putative error pattern and a dot corresponds to a flipped bit location. As presented in Fig. 3 (b) and discussed in section



Fig. 5. Checking test error patterns corresponding to a noise burst of length $1 \le l \le n$, where $s_{1,2...,l} = \boldsymbol{H} \cdot \mathbb{1}_1^\top \oplus \boldsymbol{H} \cdot \mathbb{1}_2^\top \ldots \oplus \boldsymbol{H} \cdot \mathbb{1}_l^\top$.

III-B, we propose rearranging these error patterns to simplify the hardware implementation.

The maximum number of codebook membership queries (and hence the worst-case complexity) for GRAND-MO decoding is determined by Δl , $\frac{1}{g}$, and $\frac{E_b}{N_0}$. It should be noted that the average number of codebook membership queries for GRAND and its variants is far lower than the maximum number of codebook membership queries. To reduce worstcase complexity, we suggest restricting the number of bursts mas well as burst sizes l_m for the generated test error patterns. Figure 3 (c) depicts the generation of a modified test error pattern with parameters m = 2, $l_1 = 4$ and $l_2 = 3$. In comparison to the Markov query order, the proposed query order with parameters $(m = 2, l_1 = 4 \text{ and } l_2 = 3)$ reduces the worst-case complexity from 60 to 46 test error patterns.

The FER performance for GRAND-MO decoding of BCH code (127, 106) with g = 0.2 is shown in Fig. 4. The performance of the decoder using the proposed query order with different parameters (m, l_m) , is compared to the performance of the decoder with the original Markov query order. The proposed query order with parameters $(m = 2, l_1 = 32, l_2 = 8)$ results in a 0.3 dB degradation in FER at 10^{-5} ; however, the maximum number of codebook membership queries is reduced from 3530504 queries required by Markov order to 487818 queries at $\frac{E_b}{N_0} = 8$ dB. Similarly, for RLCs, the proposed query order's parameters m and l_m can be adjusted to match the FER performance of GRAND-MO with Markov query order for different lengths, rates, and average burst lengths. Fig. 2 shows the FER performance for GRAND-MO decoding with the Markov query order and the proposed query order for RLC code (128, 104).

B. Principle, Scheduling and Details

For a (n, k) linear block code, a VLSI architecture for GRANDAB (AB=3) decoder was proposed in [12]. The proposed architecture uses $n \times (n - k)$ -bit shift registers to store (n - k)-bit syndromes of 1-bit flip error patterns ($s_i = \mathbf{H} \cdot \mathbf{1}_i^{\top}$ with $i \in [\![1 \dots n]\!]$). Moreover, the proposed decoder uses the linearity property of the underlying code to combine l 1-bit flip error syndrome to generate an error pattern with the Hamming weight of l ($s_{1,2...,l} = \mathbf{H} \cdot \mathbf{1}_1^{\top} \oplus \mathbf{H} \cdot \mathbf{1}_2^{\top} \dots \oplus \mathbf{H} \cdot \mathbf{1}_l^{\top}$). By shifting the data stored in the shift registers, error pattern



(a) Checking all test error patterns corresponding to a single noise burst of size $l \le 4$ in one time-step



(b) Error patterns corresponding to a single noise burst of size $l \leq 4$ (red-rectangle).

Fig. 6. Checking test error patterns for GRAND-MO decoding corresponding to proposed query order with parameters $(n = 6, m = 2, l_1 = 4 \text{ and } l_2 = 3)$.



(a) Checking all test error patterns corresponding to m = 2 and $l_1 = 1$ with $s_{comp} = s_c \oplus s_1$.



Fig. 7. Checking test error patterns corresponding to proposed query order for GRAND-MO at time step 2.

syndromes corresponding to different bit flip patterns are generated. This approach forms the basis for the proposed GRAND-MO architecture. Since the proposed architecture for GRANDAB [12] can only generate test error patterns with Hamming weights ≤ 3 , significant improvements are needed to support generating error patterns with burst lengths $l \geq 3$.

Fig. 5 presents the contents of the $n \times (n - k)$ -bit shift register and the associated peripheral circuitry. This structure is used to generate the test error patterns corresponding to a noise burst of length l $(1 \le l \le n)$. Each row of the shift register stores a syndrome corresponding to a noise burst, such that the l^{th} row stores the syndrome corresponding to a noise burst of length l $(s_{1,2...,l} = \mathbf{H} \cdot \mathbb{1}_1^\top \oplus \mathbf{H} \cdot \mathbb{1}_2^\top ... \oplus \mathbf{H} \cdot \mathbb{1}_l^\top)$. Through combining each row of the shift register with the syndrome of the received vector s_c $(s_c = \mathbf{H} \cdot \mathbf{r}^\top)$ using the



(a) Checking all test error patterns corresponding corresponding to m = 2 and $l_1 = 1$ with $s_{comp} = s_c \oplus s_2$.



Fig. 8. Checking test error patterns corresponding to proposed query order for GRAND-MO at time step 3.



(a) Checking all test error patterns corresponding to m = 2 and $l_1 = 2$ with $s_{comp} = s_c \oplus s_{1,2}$.



(b) Error patterns corresponding to m = 2 and $l_1 = 2$ with $s_{comp} = s_c \oplus s_{1,2}$ and n = 6 (red-rectangle).

Fig. 9. Checking test error patterns corresponding to proposed query order for GRAND-MO at time step 6.

(n-k)-bit-wide XOR gates, we can compute the syndrome of the test error patterns corresponding to a noise burst of length l. Each of the n test syndromes is NOR-reduced, to feed an n-to-log₂ n priority encoder. The output of each NOR-reduce is 1 if and only if all the bits of the syndrome computed by (1) are 0.

Based on the example presented in Fig. 3 (c), we explain the VLSI architecture for the proposed query order for GRAND-MO decoding. An example of the contents of the shift register and the arrangement of XOR gates is presented in Fig. 6. This structure is used to generate test error patterns corresponding to the proposed query order with parameters n = 6, m = 2, $l_1 = 4$ and $l_2 = 3$. For the sake of clarity, the priority encoder and its associated signals are omitted in the figure. Due to the use of a specific arrangement of shift register and XOR gates, all the error patterns corresponding to a single noise burst (m = 1) of size $l \le 4$ are checked (1) in a single time step as presented in Fig. 6 (b).

To generate the test error patterns corresponding to m > 1, a controller is used in conjunction with the shift register. Fig. 7 shows the contents of the shift register and the syndrome that is outputted by the controller, which is denoted as s_{comp} ,



Fig. 10. Proposed VLSI Architecture for GRAND-MO.

to generate test error patterns corresponding to m = 2 and $l_1 = 1$. The shift register is shifted-up by 2 positions and the controller outputs $s_{comp} = s_c \oplus s_1$. Hence, all the test error patterns with $s_{comp} = s_c \oplus s_1$ are checked in one time step. At the next time step, the controller outputs $s_{comp} = s_c \oplus s_2$ and the shift register is shifted up by 1 position. This allows us to generate all the test error patterns, with $s_{comp} = s_c \oplus s_2$ as shown in Fig. 8. Therefore, for a code length of n, n - 2 time steps are required to generate all test error patterns corresponding to m = 2 and $l_1 = 1$ where shift register is shifted up by 1 in each time step.

Similarly, to generate test error patterns corresponding to m = 2 and $l_1 = 2$, the shift register is reset and shifted-up by 3 positions. In this position, the controller outputs $s_{comp} = s_c \oplus s_1 \oplus s_2$ as shown in Fig. 9. A total number of n-3 time steps are required to generate all test error patterns corresponding to m = 2 and $l_1 = 2$ since the shift register is shifted up by 1 in each time step. In summary, for the proposed VLSI architecture, the number of required time steps to check all the error patterns corresponding to the proposed query order with parameters $(n, m = 2, L = min(l_1, l_2)])$ is given by:

$$L \times (\frac{2 \times n - L - 3}{2}) + 2.$$
 (2)

The proposed VLSI architecture for GRAND-MO is presented in Fig. 10. For clarity, the control and clock signals are not shown. The proposed architecture takes r as input and generates the estimated word as output \hat{u} . At any time, to support any code, given the length and rate constraints, an H matrix can be loaded into the H memory. To begin, a syndrome check is performed on r to determine whether the received vector is a valid codeword. If the syndrome is verified, decoding is assumed to be successful and we terminate by outputting $\hat{u} = r$. Otherwise, the *decoding core* applies test error patterns in the proposed query order until one of the test error pattern verifies the parity check constraint (1). After verifying that the resulting codeword belongs to the codebook, the controller module forwards the respective indices to the word generator module which translates these index values to their correct bit flip locations.

C. Implementation Results

The proposed GRAND-MO architecture with parameters $(m = 2, l_1 \le 32 \text{ and } l_2 \le 32)$, has been implemented in Verilog HDL and synthesized using Synopsys Design Compiler



Fig. 11. Comparison of the GRAND-MO decoding and BCH (PGZ) decoding performance for BCH code (79, 64) in Markov channels (g = 0.4).

with general-purpose TSMC 65 nm CMOS technology. The design has been verified using test benches generated via the bit-true C model of the proposed hardware. Table I presents the synthesis results for the proposed decoder with n = 128, code rates between 0.75 and 1.

The GRAND-MO implementation can support a maximum frequency of 500 MHz. Since no pipelining strategy is used. one clock cycle corresponds to one time-step. For n = 128and parameters ($m = 2, l_1 \leq 32$ and $l_2 \leq 32$) 3538 cycles (2) are required in the worst-case (W.C.) scenario, resulting in a W.C. latency of 7.0 μ s. The average latency, however, is only 2 ns at target FER of 10^{-5} , which results in an average decoding information throughput of 52 Gbps for the (128,104) RLC code presented in Fig. 2. The proposed GRAND-MO decoder has a $2.8 \times$ area overhead as compared to the hard decision-based GRANDAB decoder (AB=3) [12]. The average decoding throughput for both the proposed GRANDMO and GRANDAB decoder [12] is comparable. The proposed GRAND-MO decoder, on the other hand, has 13.6%lower W.C. latency, resulting in 13.6% higher W.C. decoding throughput. Furthermore, as seen in Fig. 2. GRAND-MO's decoding performance with parameters (q = 0.4, m = 2, $l_1 = 32$, and $l_2 = 16$) outperforms GRANDAB decoder by at least 3 dB for target FERs less than 10^{-5} .

Recently, a high throughput VLSI architecture for a (79, 64) BCH code decoder based on the Peterson-Gorenstein–Zierler

 TABLE I

 TSMC 65 NM CMOS IMPLEMENTATION COMPARISON FOR GRANDAB

 WITH GRAND-MO FOR n = 128.

GRANDAB [12]	GRAND-MO
AB = 3	$m = 2, l_1 \leq 32 \text{ and } l_2 \leq 32$
65	65
0.9	0.9
500	500
0.25	0.71
8196	7076
2	2
12.68	14.69
52	52
Yes	Yes
Yes	Yes
	$\begin{tabular}{ c c c c c } \hline & GRANDAB [12] \\ \hline & AB = 3 \\ & 65 \\ & 0.9 \\ & 500 \\ & 0.25 \\ & 8196 \\ & 2 \\ & 12.68 \\ & 52 \\ & 12.68 \\ & 52 \\ & Yes \\ & Yes \\ \hline \end{tabular}$

TABLE II

TSMC 65 NM CMOS IMPLEMENTATION COMPARISON FOR BCH decoder with GRAND-MO $(m=1,l_1\leq 16 \text{ and } l_2=0)$ for n=79.

	GRAND-MO	(79,64) BCH decoder [13]
Technology (nm)	65	65
Supply (V)	1.1	1.2
Max. Frequency (GHz)	1	N/A
Area (μm^2)	225 964	3 264
W.C. Latency (ns)	2	3
Avg. Latency (ns)	1	1.1
W.C. T/P (Gbps)	32	21.3
Avg. T/P (Gbps)	64	58.2
Code compatible	Yes	No
Rate compatible	Yes	No

(PGZ) algorithm [19] was proposed in [13]. The decoding performance of the (79,64) BCH PGZ decoder is compared with that of GRAND-MO decoding in Fig. 11. As seen in Fig. 11, GRAND-MO with proposed query order and parameters $(m = 1, l_1 = 16 \text{ and } l_2 = 0)$ outperforms BCH decoder by 2 dB for target FER of 10^{-5}

Table II compares the implementation results for GRAND-MO (m = 1, $l_1 \leq 16$, and $l_2 = 0$) and the BCH decoder in [13]. For n = 79 and (m = 1, $l_1 = 16$, and $l_2 = 0$), 2 cycles (2) are required in the W.C. scenario. Even though the proposed decoder is $69 \times$ bigger than the PGZ decoder in [13], the W.C. latency is reduced by 33% resulting in a W.C throughput of 32 Gbps. For target FER of 10^{-5} , the proposed decoder exhibits a slightly better minimum latency and achieves an information throughput of 64 Gbps, while the BCH decoder is limited to 58 Gbps. In addition, the proposed GRAND-MO architecture can decode any code with n = 79and $R \geq 0.75$, while [13] can only decode the (79,64) BCH code.

IV. CONCLUSION

In this paper, we propose the first hardware architecture for the GRAND-MO algorithm. GRAND-MO is a GRAND variant that is used to decode linear block codes on communication channels with memory. Since GRAND is code-agnostic, the proposed GRAND-MO architecture will decode any error correcting code provided the length and rate constraints. We suggest modifications in the GRAND-MO algorithm to simplify the hardware implementation and reduce the complexity of the decoding process. The results of ASIC synthesis show that with a code length of 128 and a target FER of 10^{-5} , an average information throughput of 52 Gbps and a 3 dB gain in decoding performance can be achieved when compared to the GRANDAB (AB=3) decoder. Moreover, compared with the BCH decoder tailored for a (79,64) code, the proposed VLSI implementation achieves 33% higher worst-case throughput while also providing a 2 dB gain in decoding performance for a target FER of 10^{-5} . In addition to that, the average throughput for the same parameters can reach up to 64 Gbps. This proposed architecture paves the way for future soft-input GRAND-MO implementations.

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